

ABSTRACT OF THE DISCLOSURE

A digital signal processor capable of performing a Viterbi algorithm is provided. The digital signal processor includes an instruction fetching unit that fetches instructions, a decoding unit that decodes the instructions fetched by the instruction fetching unit; and an execution unit that executes the instructions decoded by the decoding unit. The execution unit includes an arithmetic logic unit configured to perform a register-register arithmetic logic operation. The arithmetic logic unit compares a first data with a second data, in parallel with a comparison of a third data with a fourth data. The first data, the second data, the third data, and the fourth data can each be one of four results obtained by adding one of two path metrics to one of two branch metrics. The execution unit outputs new path metrics.